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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/930,857	08/15/2001	Brad A. Davis	BEA920010010US1	2098

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EXAMINER	
CHEN, ALAN S	

ART UNIT	PAPER NUMBER
2182	4

DATE MAILED: 07/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/930,857	DAVIS ET AL.	
	Examiner	Art Unit	
	Alan S Chen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 4, 5, 17 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 4 and 17 recites the limitation "renumbering nodes in an existing hardware resource map" in line 1 and 2 of claim 4. There is insufficient antecedent basis for this limitation in the claim. "Nodes" were not specified and can be interpreted to mean any components in a computer system, e.g., RAM, hard disk, etc. The independent claims from which these claims depend do not distinguish what nodes are. For instance, they reference a "computer system", which in and of itself can be considered a node, or all the components in a single "computer system" can be considered nodes.

4. Claim 5 and 18 are rejected based on a rejected base claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. Claims 1-4,6,7 and 33 are rejected under 35 U.S.C. 102(e) as being anticipated by No. 6,446,188 to Henderson et al. (hereafter Henderson).

7. As per claim 1, Henderson discloses a method for accessing hardware resources in a computer system (Fig. 3), comprising: assigning a first I/O resource a first physical resource address (Fig. 3A, element 308A and its associated physical address in Fig. 3A, element 306), Henderson discloses these as objects used by the processor, I/O commands/references, inherently part of what the processor uses in interacting with its memory devices); assigning a second I/O resource a second physical address (Fig. 3A, element 308C and its associated physical address in Fig. 3A, element 306); dynamically routing a virtual resource address between said first and second physical resource addresses (as seen literally in the object cache, Fig. 3A, element 210, the virtual object 2 sits between object 3 and object 1, each having a unique physical address in Fig. 3A, element 306. Also, in another view, the physical address of object 2 can clearly lay between the physical address in object 1 and object 3 in the physical system memory, element 306).

8. As per claims 2 and 33, Henderson discloses claim 1, wherein the step of dynamically routing said virtual resource address includes providing a hardware resource map for logically storing said virtual resource address and at least one of said first and second physical resources addresses (Fig. 5, element 418).

9. As per claim 3, Henderson discloses claim 1, wherein the step of dynamically routing said virtual resource address includes redirecting said virtual resource address from said first physical resource address to said second physical resource address (Column 5, lines 35-39,

where if there is a miss, management table will be modified to prevent the miss, so if the node being a memory device has a miss, then rerouting to another memory device).

10. As per claim 4, Henderson discloses claim 3, further comprising renumbering nodes in an existing hardware resource map (this is inherent since the physical address space spans across multiple devices, nodes, etc, and the repointing of a virtual-to-physical address requires the physical address to have some indication of where the particular node exists).

11. As per claim 6, Henderson discloses claim 1, Henderson discloses the step of dynamically routing said virtual resource address includes changing a hardware resource map at runtime (Fig. 3A, virtual to physical address associations are dynamic and not only during initialization).

12. As per claim 7, Henderson discloses claim 1, wherein the physical resource address are on different nodes of a computer system (Column 4, lines 30-45, various memory devices can exist, these being considered different nodes in the computer system).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 14-17, 27 and 28-32 are rejected under 35 USC 103(a) as being unpatentable over Henderson in view of No. 6,314,501 to Gulick et al. (hereafter Gulick).

15. As per claim 14 and 27, Henderson discloses a computer system and article comprising a first I/O resource having a first physical resource address (Fig. 3A, element 308A and its

associated physical address in Fig. 3A, element 306), Henderson discloses these as objects used by the processor, I/O commands/references, inherently part of what the processor uses in interacting with its memory devices); a second I/O resource having a second physical resource address (Fig. 3A, element 308C and its associated physical address in Fig. 3A, element 306); and a manager to translate said virtual address to one of said first and second physical resource addresses (Fig. 3A, element 208 as seen literally in the object cache, Fig. 3A, element 210, the virtual object 2 sits between object 3 and object 1, each having a unique physical address in Fig. 3A, element 306. Also, in another view, the physical address of object 2 can clearly lay between the physical address in object 1 and object 3 in the physical system memory, element 306).

Henderson does not disclose expressly a platform having a virtual resource address and a physical resource address.

Gulick discloses the ability to use firmware in network architecture involving address mapping (Column 60, lines 53-63) in a multi-processor environment with a system interconnect (Fig. 1)

Henderson and Gulick are analogous art because they are from the similar problem solving area in address remapping.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Henderson and Gulick to embrace a multiprocessor environment.

The suggestion/motivation for doing so would have been to accommodate the demands of the user as modern computer systems grow and require more processing power, leading to the inevitable use of multiple processor nodes and multiple operating systems (Column 2, lines 32-40). Using firmware to implement many of the functions of the system is a design choice. The

advantages or using firmware is clear in that it is generally faster than a software implementation while allowing the designer to reprogram it.

Therefore, it would have been obvious to combine Henderson with Gulick for the benefit of scaling the processing power by incorporating multiple computer systems and using firmware to speed up the processing done outside the processor.

16. As per claims 15 and 16, Henderson combined with Gulick discloses claim 14, wherein Henderson further discloses having a hardware resource map to logically store said virtual address and at lest one of said first and second physical resource addresses as well as redirecting virtual to physical addresses (Fig. 3A, element 310).

17. As per claim 17, Henderson combined with Gulick discloses claim 16, wherein Henderson further discloses renumbering nodes in an existing hardware resource map (this is inherent since the physical address space spans across multiple devices, nodes, etc, and the repointing of a virtual-to-physical address requires the physical address to have some indication of where the particular node exists).

18. As per claim 28, Henderson combined with Gulick discloses claim 27, wherein Henderson further discloses the medium is selected from a group consisting of a recordable data storage medium, and a modulated carrier signal (Fig. 3A, elements 102 and element 306 are store data and the signals are inherently modulated in that they are changing signals that correspond to particular values of digital data at a particular time).

19. As per claim 29, Henderson combined with Gulick discloses claim 27, Henderson further disclosing wherein said logical storing means is a hardware resource map (Fig. 3A, element 208).

20. As per claim 30, Henderson combined with Gulick discloses claim 27, Henderson further disclosing a manager to translate said resource address and to redirect said virtual address to a physical hardware address (Fig. 3A, element 102).

21. As per claim 31, Henderson combined with Gulick discloses claim 30, Henderson further disclosing dynamic routing means comprises an instruction for renumbering nodes in said logical storing means (this is inherent since the physical address space spans across multiple devices, nodes, etc, and the repointing of a virtual-to-physical address requires the physical address to have some indication of where the particular node exists).

22. As per claim 32, Henderson combined with Gulick discloses claim 27, Henderson further disclosing wherein said dynamic routing means comprises an instruction to change said logical storing means at run time (Fig. 3A, virtual to physical address associations are dynamic and not only during initialization).

23. Claims 8-13 and 19-26 are rejected under 35 USC 103(a) as being unpatentable over Henderson in view of Gulick.

Henderson combined with Gulick discloses claim 1.

Henderson does not disclose expressly a multiprocessor system where dynamically routing virtual address includes mapping virtual to physical addressing uses firmware and details pertaining to the system interconnect.

Gulick discloses the ability to use firmware in network architecture involving address mapping (Column 60, lines 53-63) in a multi-processor environment with a system interconnect (Fig. 1).

Henderson and Gulick are analogous art because they are from the similar problem solving area in address remapping.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Henderson and Gulick to embrace a multiprocessor environment.

The suggestion/motivation for doing so would have been to accommodate the demands of the user as modern computer systems grow and require more processing power, leading to the inevitable use of multiple processor nodes and multiple operating systems (Column 2, lines 32-40). Using firmware to implement many of the functions of the system is a design choice.

Therefore, it would have been obvious to combine Henderson with Gulick for the benefit of scaling the processing power by incorporating multiple computer systems.

Allowable Subject Matter

24. Claims 5 and 18 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to single and multiprocessor address mapping methodologies:

U.S. Pat. No. US006212613B1 to Belair

U.S. Pat. No. US 20020103943A1 to Lo et al.

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S Chen whose telephone number is 703-605-0708. The examiner can normally be reached on M-F 8:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on 703-308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ASC
07/12/2004

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